TITLE OF THE INVENTION

CMOS IMAGE SENSOR AND MANUFACTURING METHOD OF THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a CMOS image sensor composed of a photodiode and a MOS transistor, which are formed on a semiconductor substrate and a manufacturing method of the same.

2. Description of the Prior Art

Recently, a CMOS image sensor has been widely used as a solid state imaging device. The CMOS image sensor has various kinds of advantages that it consumes less power compared to CCDs (Charge Coupled Device), can be driven by a single power source, and can fabricate peripheral circuits such as a timing generating circuit, a reading-out circuit and an A/D converter unitedly.

Fig. 1 is an equivalent circuit diagram for one pixel of the CMOS image sensor. One pixel of the CMOS image sensor shown in Fig. 1 is composed of one photodiode PD, three N-channel MOS transistors T1, T2, and T3. The cathode of the photodiode PD is connected to the drain of the transistor T1 and the gate of the transistor T2. The sources of the transistors T1 and T2 are connected to a power supply line to which a reference voltage VR is supplied. Moreover, the gate of the transistor T1 is connected to a reset line to which a

reset signal RST is supplied.

The source of the transistor T3 is connected to the drain of the transistor T2, and the drain of the transistor T3 is connected to a reading-out circuit (not shown) through a signal line. The gate of the transistor T3 is connected to a column selection line to which a select signal SLCT is supplied.

The transistor T1 is called a reset transistor, and the transistor T2 is called a drive transistor. Moreover, the transistor T3 is called a selection transistor.

In the CMOS image sensor, a plurality of pixels which are illustrated by the equivalent circuit in Fig. 1 are arranged in horizontal and vertical directions in a semiconductor substrate, and peripheral circuits such as a reading-out circuit and an A/D (analog digital) conversion circuit are formed outside a region where the plurality of pixels are formed.

Note that in Japanese Patent Laid-Open No. 10(1988)-248035, disclosed is a driving method in which a potential of a signal supplied to a gate of a reset transistor is allowed to change in three stages, and a dynamic range of a CMOS image sensor is widened.

By the way, when the circuit shown in Fig. 1 is formed on a semiconductor substrate, it is necessary to connect electrically a source/drain of a MOS transistor formed on the semiconductor substrate and a wiring formed

on the semiconductor substrate with an insulating film therebetween. When a contact hole is formed in the insulating film and a conductive substance is buried in the contact hole, simply, a contact resistance between the conductive substance and the source/drain is large. Although it is conceived to make the resistivity low by forming a silicide film on a surface of the source/drain of the MOS transistor and connecting electrically the source/drain and the wiring with the silicide film therebetween, leak current increases at a connection portion of the reset transistor and the photodiode with such structure, thus causing deterioration in characteristics. Note that the leak current includes a periphery length component which leaks at an edge portion of a field oxide film and an area component which leaks at a PN junction portion. The cause of the leak at the periphery length component is considered as follows. Injection ions are absorbed in the silicide at a portion where a concentration of the injection ions of the edge of the field oxide film is presumed to be low, and hence the ion concentration becomes lower. Moreover, the area component is considered to be increased because a depletion layer is contaminated with metal atoms in forming the silicide.

SUMMARY OF THE INVENTION

The object of the present invention is to provide

a CMOS image sensor which suppresses leak current at a drain portion of a reset transistor by reducing a resistivity between source/drain of a MOS transistor and a wiring, and a manufacturing method of the same.

The CMOS image sensor of the present invention composed of a photodiode having an impurity region formed in a semiconductor substrate, and a first and a second MOS transistors formed by introducing impurities into the semiconductor substrate, wherein no silicide film exists on surface of impurity regions of the first MOS transistor disposed at least on a side of the photodiode, the impurity region being connected to an impurity region of the photodiode, and the silicide film is provided on surfaces of impurity regions of the second MOS transistor.

In the present invention, the silicide film is not formed on the impurity region (source or drain) of the first MOS transistor (reset transistor) which is connected to the photodiode and disposed on the side of the photodiode. Therefore, an increase in a leak current owing to metal atoms is prevented, and the CMOS image sensor showing less noise can be obtained.

Furthermore, in the present invention, the silicide film is formed on the impurity region of the second MOS transistor. Then, the wiring and the impurity region are electrically connected so as to interpose the silicide film therebetween. Thus, a contact resistance between the wire and the impurity region becomes low, and

deterioration of electrical characteristics can be avoided.

The manufacturing method of the CMOS image sensor of the present invention comprises the steps of: forming a photodiode by introducing impurities into a semiconductor substrate; forming a gate electrode on the semiconductor substrate so as to interpose a gate insulating film therebetween; forming a plurality of N channel MOS transistors by introducing N type impurities into the semiconductor substrate, the N channel MOS transistors including a reset transistor having an N type impurity region connected to a cathode of the photodiode; forming a first insulating film covering a region extending at least from the photodiode to an impurity region on one side of the reset transistor positioned on one side of the photodiode; and forming a metal film above the semiconductor substrate and allowing metal in the metal film and silicon on a surface of the silicon substrate to react with each other, thus forming a silicide film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an equivalent circuit diagram of one pixel of a CMOS image sensor.

Fig. 2 is a block diagram of a CMOS image sensor of an embodiment according to the present invention.

Fig. 3 is a plan view showing one pixel of the

CMOS image sensor thereof.

Figs. 4A to 4C are diagrams showing a manufacturing method of a CMOS image sensor of an embodiment, and section views (No. 1) of formation portions of a photodiode and a reset transistor.

Figs. 5A to 5C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 2) of formation portions of the photodiode and the reset transistor.

Figs. 6A to 6C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 3) of formation portions of the photodiode and the reset transistor.

Figs. 7A to 7C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 4) of formation portions of the photodiode and the reset transistor.

Figs. 8A to 8C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 5) of formation portions of the photodiode and the reset transistor.

Figs. 9A to 9C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 6) of formation portions of the photodiode and the reset transistor.

Figs. 10A to 10C are diagrams showing the manufacturing method of the CMOS image sensor of the

embodiment, and section views (No. 7) of formation portions of the photodiode and the reset transistor.

Figs. 11A to 11C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 8) of formation portions of the photodiode and the reset transistor.

Figs. 12A to 12C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 1) of a peripheral CMOS circuit formation portion.

Figs. 13A to 13C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 2) of a peripheral CMOS circuit formation portion.

Figs. 14A to 14C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 3) of a peripheral CMOS circuit formation portion.

Figs. 15A to 15C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 4) of a peripheral CMOS circuit formation portion.

Figs. 16A to 16C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 5) of a peripheral CMOS circuit formation portion.

Figs. 17A to 17C are diagrams showing the

manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 6) of a peripheral CMOS circuit formation portion.

Figs. 18A to 18C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 7) of a peripheral CMOS circuit formation portion.

Figs. 19A to 19C are diagrams showing the manufacturing method of the CMOS image sensor of the embodiment, and section views (No. 8) of a peripheral CMOS circuit formation portion.

Fig. 20 is a plan view showing a CMOS image sensor of a comparison example.

Fig. 21 is a timing chart showing an operation of the CMOS image sensor of the embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described with reference to the accompanying drawings below.

Fig. 2 is a block diagram of a CMOS image sensor of an embodiment of the present invention, and Fig. 3 is a plan view showing one pixel of the CMOS image sensor thereof.

As shown in Fig. 2, a light receiving portion 1, a reading-out circuit 2, a timing generating circuit 3, an A/D converter 4 and the like are formed on a silicon

semiconductor substrate 10. A plurality of pixels are formed in the light receiving portion 1 so as to be arranged. One pixel is composed of one photodiode PD and three N channel MOS transistors T1, T2, and T3 as shown in Fig. 3, and an equivalent circuit thereof is illustrated by Fig. 1. Moreover, the circuits such as the reading-out circuit 2, the timing generating circuit 3 and the A/D converter 4 are constituted of CMOS transistors.

Figs. 4 to 19 are drawings showing a manufacturing method of the CMOS image sensor of the embodiment of the present invention. Note that Figs. 4 to 11 are section views of portions of the photodiode and the reset transistor T1, and Figs. 12 to 19 are section views in a CMOS circuit portion of a peripheral circuit.

First, as shown in Fig. 4A and Fig. 12A, a surface of the silicon semiconductor substrate 10 is thermally oxidized and a silicon oxide film (not shown) having a thickness of about 3 nm is formed, and thereafter a silicon nitride film (SiN film) 11 is formed to a thickness of about 115 nm thereon. Then, a resist film 12 having an opening portion at a portion corresponding to a field oxide film formation portion is formed on the silicon nitride 11, and the silicon nitride film 11 is etched using the resist film 12 as a mask. Thereafter, the resist film 12 is removed.

SUB A1

Next, as shown in Fig. 4B and Fig. 12B, the

SUB A1

entire surface of the resultant structure is coated with a photoresist film 13 so as to cover the silicon nitride film 11, and an opening portion is provided at a portion corresponding to a P channel MOS transistor formation portion after exposure and developing steps. Phosphorus (P) is ion-injected to the semiconductor substrate 10 through the opening portion under conditions of, for example, 180 keV and 1.4 × 1013/cm2, and an N type impurity region 41 is formed.

Thereafter, as shown in Fig. 4C and Fig. 12C, the resist film 13 is removed, and a thermal treatment is performed at a temperature of 1150 ℃ so as to diffuse the impurities. Thus, an N well 42 is formed in the P channel MOS transistor formation portion.

Next, as shown in Fig. 5A and Fig. 13A, a thermal treatment is performed at a temperature of 900 ℃, and a field oxide film 16 having a thickness of about 370 nm is formed at a portion that is not covered with the silicon nitride film 11. Thereafter, the silicon nitride film 11 is removed.

SUB A2

Subsequently, a well of a photodiode formation portion is formed. Specifically, boron (B) is ion-injected to the whole of a light receiving portion under conditions of, for example, 600 keV and 3×1012/cm2, and a P type impurity layer (well) 43 is formed in the semiconductor substrate 10.

SUB A3

Thereafter, as shown in Fig. 5C and Fig. 13B, the

SUB A3

photodiode formation portion and the P channel MOS transistor formation portion are covered with a resist film 17, and boron (B) is ion-injected to an N channel MOS transistor formation portion under conditions of, for example, 140 keV and 8 × 1012/cm2, and a P well 44 is formed. At the same time, a channel stopper layer 44a of an N channel MOS transistor. Thereafter, the resist film 17 is removed.

Next, as shown in Fig. 6A and Fig. 13C, a silicon oxide film (gate oxide film) 18 having a thickness of about 7 nm is formed on a surface of the semiconductor substrate 10 by performing a thermal treatment at temperature of 800 ℃. Then, an amorphous silicon film 19 is formed on the entire surface of the resultant structure to a thickness of about 50 nm by a CVD (Chemical Vapor Deposition) method.

Thereafter, as shown in Fig. 6B, a resist film 20 is selectively formed on the amorphous silicon film 19 of the photodiode formation portion. Thereafter, boron (B) is ion-injected to a portion of the semiconductor substrate 10 that is not covered with the resist film 20 under conditions of, for example, 30 keV and 1.8 × 1012/cm2. This ion-injection is performed so as to adjust thresholds of the N and P channel MOS transistors. Thereafter, the resist film 20 is removed.

SUB A4

Next, as shown in Fig. 6C and Fig. 14A, a WSi (tungsten silicon) film 21 is grown on the amorphous film

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19 to a thickness of 150 nm. Then, the phosphorus (P) is ion-injected under conditions of, for example, 40 keV and 8 × 1015/cm2, thus converting the amorphous silicon film 19 to a low resistance substance.

Subsequently, as shown in Fig. 7A and Fig. 14B, a silicon oxide film 22 is formed on the WSi film 21 to a thickness of about 45 nm by the CVD method. On the silicon oxide film 22, formed is an amorphous carbon film (not shown) as a reflection prevention layer to a thickness of about 32 nm by a PVD (Physical Vapor Deposition) method.

SUB A5

Thereafter, as shown in Fig. 7B and Fig. 14C, the amorphous carbon film, the silicon oxide film 22, the WSi film 21, the amorphous silicon film 20 and the silicon oxide film 18 are etched by photolithography, and gate electrodes of the MOS transistors are formed.

Next, as shown in Fig. 7C, a resist film 23 having an opening portion is formed in the photodiode formation portion, and then phosphorus (P) is ion-injected to the photodiode formation portion under conditions of, for example, 20 keV and 4 × 1015/cm2, thus forming an N type impurity region 45. Thereafter, the resist film 23 is removed, and a thermal treatment is carried out at a temperature of 1000 ℃ and for 10 seconds.

SUB A6

Subsequently, as shown in Fig. 8A and Fig. 15A , a resist film 25 that covers the P channel MOS transistor formation portion and a photodiode formation portion is

SUB A6

formed, and phosphorus (P) is ion-injected to both sides of the gate electrode of the N channel MOS transistor formation portion under conditions of, for example, 20 keV and $4 \times 1013/cm2$, thus, forming a low concentration N type impurity region 46. Thereafter, the resist film 25 is removed.

Next, as shown in Fig. 8B and Fig. 15B, a resist film 26 that covers the N channel MOS transistor formation portion and the photodiode formation portion is formed, and BF2 is ion-injected to both sides of the gate electrode of the P channel MOS transistor formation portion under conditions of, for example, 20 keV and 1013/cm2, thus forming a low concentration P type impurity region 47. Thereafter, the resist film 26 is removed.

Subsequently, as shown in Fig. 8C and Fig. 15C, on the entire surface of the resultant structure, formed is a silicon oxide film 27 to a thickness of 120 nm. Then, a photoresist film 28 is formed on the silicon oxide film 27, and a portion serving as a silicide block is patterned. In this embodiment, the portion shown by the dotted lines in Fig. 3, that is, the portion extending from the photodiode formation portion to the drain of the reset transistor T1 is covered with the resist film 28.

Next, as shown in Fig. 9A and Fig. 16A, a side wall 29 is formed on the side portion of the gate

electrode by performing anisotropic etching for the silicon oxide film 27. Thereafter, the resist film 28 is removed.

SUB A7 5

Subsequently, as shown in Fig. 16B, a resist film 30 that covers a portion other than P channel MOS transistor formation portion is formed, and BF2 is ion-injected to both sides of the gate electrode of the P channel MOS transistor under conditions of, for example, 20 keV and 3×1015/cm2, thus forming a high concentration P type impurity region 48. Thereafter, the resist film 30 is removed.

Furthermore, as shown in Fig. 9B and Fig. 16C, a resist film 31 that covers the P channel MOS transistor formation portion is formed, and arsenic (As) is ion-injected to both sides of the gate electrode of the N channel MOS transistor under conditions of, for example, 30 keV and 1015/cm2, thus forming a high concentration P type impurity region 49. Thereafter, the resist film 31 is removed. Then, the P type channel impurity region 48 and the N type impurity region 49 are activated by performing a thermal treatment at 1000 ℃ and for 10 seconds. Thus, an N channel MOS transistor and a P channel MOS transistor having an LDD structure are completed. Note that though the drain side of the reset transistor T1 (a side connected to the photodiode) is not formed to the LDD structure, it was confirmed by experiments performed by the inventors of this

SUB A7

application that any trouble is not brought about practically even if this side is formed to the LDD structure.

Next, as shown in Fig. 9C and Fig. 17A, Ti is sputtered on the entire surface of the resultant structure, thus forming a Ti film 32 having a thickness of 30 nm. Then, a thermal treatment is performed at a temperature of 700 ℃ and for 90 seconds, and a portion of the Ti film 32 contacting the semiconductor substrate 10 is converted to silicide.

Thereafter, as shown in Fig. 10A and Fig.17B, an unreacted portion of the Ti film 32 is removed by etching. By this etching, a silicide film 33 is left on surfaces of source/drain regions of the MOS transistor. After that, a thermal treatment is performed at a temperature of 800 ℃ and for 30 seconds, thus stabilizing the silicide film 33.

SUB A8

Next, as shown in Fig. 10B and Fig. 17C, an insulating film 34 is formed on the entire surface of the resultant structure. This insulating film 34 is formed by laminating, for example, SiON having a thickness of 200 nm and, for example, SiO2 having a thickness of 300 nm. Thereafter, the insulating film 34 is coated with an SOG (Spin On Glass) film 35, thus flattening the surface of the resultant structure.

Subsequently, a photoresist film (not shown) is formed on the SOG film 35, and an opening portion is

provided in a contact hole formation portion after exposure and developing steps. Then, the SOG film 35 and the insulating film 34 are etched through this opening portion, and a contact hole 35a reaching the impurity region 46 that is the drain of the reset transistor and the predetermined silicide film 33 is formed as shown in Fig. 10C and Fig. 18A. Thereafter, the resist film is removed.

Next, as shown in Fig. 11A and Fig. 18B, Ti and TiN are formed to thicknesses of 20 nm and 50 nm on the entire surface of the resultant structure by sputtering, respectively, thus forming a Ti film 36. Thereafter, as shown in Fig. 11B and Fig. 18C, a tungsten (W) film 37 is formed to a thickness of 800 nm on the Ti film 36, thus burying the contact hole 35a with the tungsten.

Thereafter, as shown in Fig. 19A, a portion of the tungsten film 37 other than the contact hole 35a is removed by performing CMP (Chemical Mechanical Polishing) for the tungsten film 37. Thus, a tungsten plug 37a is formed. Then, Ti and TiN are formed to thicknesses of 20nm and 50 nm, respectively, and AlCu, Ti and TiN are respectively formed to thicknesses of 500nm, 5nm and 100 nm thereon. Thus, a conductive film 38 is formed.

Next, as shown in Fig. 11C and Fig. 19B, the conductive film 38 is patterned, thus forming a predetermined wiring 39. In such manner as described above, the CMOS image sensor of this embodiment is

completed.

In the CMOS image sensor formed in the above-described manner, since electrical connections of the source/drain of the transistors with the wiring are made at the positions other than the drain of the reset transistor T1 through the silicide film 33, a contact resistance at the connection portion is low. Furthermore, since a silicide film is not provided in the drain portion of the reset transistor T1 directly connected to the photodiode PD, an increase in leak current owing to metal atoms is prevented, and a S/N ratio is increased.

Fig. 21 is a timing chart showing an operation of the CMOS image sensor of this embodiment. A reset signal RST is a signal that becomes high level in a constant cycle. When the reset signal RST becomes high level, a potential on the cathode side of the photodiode PD, which is a potential at the portion corresponding to the portion shown by the point A in Fig. 1, becomes equal to a constant voltage (VR). Thereafter, when light reaches the photodiode PD after the reset signal RST becomes low level, charges in accordance with an intensity of the light are generated in the photodiode PD. The charges generated change the potential at the point A, that is, the gate voltage of the transistor T2. When a select signal SLCT becomes high level, an electric signal in accordance with the potential at the point A at that time is transmitted to a reading-out circuit (peripheral

circuit) through the transistor T3. In such manner, the signal in accordance with the intensity of the light that reached the photodiode PD is transmitted to the peripheral circuit.

Results obtained by examining influences of the leak current after manufacturing actually the CMOS image sensor according to the above-described method will be described below. The CMOS image sensor was manufactured by the above-described method as an example. Also a CMOS image sensor as a comparison example was manufactured in the same manner as that of the embodiment other than formation of the silicide film on a surface of the drain of the reset transistor T1. In the CMOS image sensor of the comparison example, only a photodiode formation portion (portion shown by the dotted lines in Fig. 20) is covered with a silicon oxide film in a silicide film formation step, as shown in Fig. 20.

Although a peripheral leak current component and an area leak current component cannot be measured directly, the leak current can be estimated depending on an output from an A/D converter. Specifically, the CMOS image sensor is driven in a dark portion, and a threshold is set to an output code of the A/D converter. Levels of the leak currents can be compared by generation frequencies of signals larger than the threshold. To be concrete, the generation frequencies of signals showing an output code of the A/D converter, which is equal to

500 (equivalent to 500 mV) or more, were examined. As a result, while the generation frequency was several tens (a sampling time of the A/D converter was 26 msec) in the CMOS image sensor of the comparison example, the generation frequency in the CMOS image sensor of this embodiment was zero to several. From this fact, it was confirmed that the CMOS image sensor of this embodiment shows less leak current compared to the CMOS image sensor of the comparison example. Furthermore, a silicide film is not formed in the drain portion of the reset transistor T1 in the CMOS image sensor of this embodiment, and a contact resistance is considered to be somewhat high. However, the CMOS image sensor operates normally, and it was confirmed that the CMOS image sensor has no trouble practically. In the CMOS image sensor of this embodiment, since the silicide film is provided in the source/drain other than the drain portion of the reset transistor T1, the CMOS image sensor of this embodiment has the same transistor parameters as those of the CMOS image sensor of the comparison example, and there is no problem in designing and using the CMOS image sensor.

Note that the CMOS image sensor of the present invention is not limited to the one in which the gate voltage of the reset transistor is changed in the two stages of low and high level, and can be applied also to the one which is driven by changing the gate voltage in three or more stages.

As described above, since the silicide film is not formed on the impurity region (the source or drain) connected to the photodiode in the side of the photodiode of the MOS transistor (the reset transistor) in the CMOS image sensor of the present invention, an increase in the leak current owing to the metal atoms is prevented, and noises are reduced. Moreover, since the silicide film is formed on the impurity regions of the MOS transistors other than the reset transistor and the wiring and each of the impurity regions are electrically connected to each other through the silicide film, the contact resistance between the wiring and the impurity region is low, and lowering of electric characteristics can be avoided.